LOCKHEED MARTIN

TECHNICAL AND COSMETIC SPECIFICATIONS

FOR

CCD485

APRIL 5, 1998

FEATURES

- 4096 x 4097 Photosite Array
- 15µm x 15µm Pixel Size
- 61.20 mm x 61.21 Active Image Area
- 4080 x 4081 Optically Active Pixels
- Near 100 % Fill Factor
- Multi-Pinned Phase (MPP) Option
- Low Readout Noise
- Wide Dynamic Range
- Three Phase Buried Channel NMOS

PERFORMANCE CHARACTERISTICS: (MPP MODE) $T_P = 25\,^{o}C$ (Notes 1 & 2)

SYMBOL	PARAMETER	RANGE			UNIT	CONDITION
		MIN	TYPICAL	MAX		
DS_{AVE}	Dark Signal, (Readout)		2.5	15	mV	Note 3
I_{DARK}	Dark Current Density (Integration)		25	100	pA/cm^2	Note 3
DSNU	Dark Signal Non-Uniformity		5	10	mV	Note 4
Q_{Sat}	Full Well Capacity	60	90		Ke^-	
V_{Sat}	Saturation Voltage	120	215		mV	
PRNU	Photoresponse Nonuniformity			10	% of V_{sat}	Note 5
CTE (V)	Charge Transfer Efficiency, Vertical	.99999	.999995		Per Phase Transfer	
CTE (H)	Charge Transfer Efficiency, Horizontal	.99995	.999995		Per Phase Transfer	
R	Responsivity		1.0		$V/\mu J/cm^2$	
S_{SF}	Sensitivity (Scale Factor)	2.0	2.5		$\mu V/e^-$	

PERFORMANCE CHARACTERISTICS: (NON-MPP MODE) $T_P = 25\,^{o}C$ (Note 1 & 2)

SYMBOL	PARAMETER	RANGE			UNIT	CONDITION
		MIN	TYPICAL	MAX		
I_{DARK}	Dark Current Density		2		nA/cm^2	Note 3
Q_{Sat}	Full Well Capacity		400		Ke^-	
V_{Sat}	Saturation Voltage		1,000		mV	

DC CHARACTERISTICS: T_P = 25 °C (Note 1)						
SYMBOL	PARAMETER	RANGE			UNIT	CONDITION
		MIN	TYPICAL	MAX		
V_{DD}	DC Supply Voltage	17	20	23	Volts	
V_{RD}	Reset Drain Voltage	12	14	16	Volts	
V_{OG}	Output Gate Voltage	0	1	5	Volts	
V_{SS}	Substrate Ground	0	0	0	Volts	
V_{RT}	Output Amplifier Return	0	3	5	Volts	

CLOCK CHARACTERISTICS: (MPP MODE) T_P = 25 °C (Note 1)						
SYMBOL	PARAMETER	RANGE			UNIT	CONDITION
		MIN	TYPICAL	MAX		
$V_{\phi H(1,2,3)}$ HIGH	Horizontal Transport Clock HIGH	+ 2	+ 5	+ 8	Volts	
$V_{\phi H(1,2,3)}$ LOW	Horizontal Transport Clock LOW	- 8	- 5	0	Volts	
$V_{\phi SG}$ HIGH	Summing Gate Clock HIGH	+ 2	+ 5	+ 8	Volts	
$V_{\phi SG}$ LOW	Summing Gate Clock LOW	- 8	- 5	0	Volts	
$V_{\phi V(1,2,3)}$ HIGH	Vertical Transport Clocks HIGH	0	+ 3	+ 6	Volts	
$V_{\phi V(1,2,3)}$ LOW	Vertical Transport Clocks LOW	- 10	- 8	- 5	Volts	
$V_{\phi R}$ HIGH	Reset Gate Clock HIGH	+ 6	+ 10	+ 14	Volts	
$V_{\phi R}$ LOW	Reset Gate Clock LOW	- 4	0	+ 2	Volts	
$V_{\phi VTG}$ HIGH	Vertical Transfer Gate Clock HIGH	0	+ 3	+ 6	Volts	
$V_{\phi VTG}$ LOW	Vertical Transfer Gate Clock LOW	- 10	- 8	- 5	Volts	

CLOCK CHARACTERISTICS: (NON-MPP MODE) T_P = 25 °C (Note 1)						
SYMBOL	PARAMETER	RANGE			UNIT	CONDITION
		MIN	TYPICAL	MAX		
$V_{\phi H(1,2,3)}$ HIGH	Horizontal Transport Clock HIGH	2	+ 5	+ 8	Volts	
$V_{\phi H(1,2,3)}$ LOW	Horizontal Transport Clock LOW	- 8	- 5	0	Volts	
$V_{\phi V(1,2,3)}$ HIGH	Vertical Transport Clocks HIGH	+ 5	+ 9	+ 15	Volts	
$V_{\phi V(1,2,3)}$ LOW	Vertical Transport Clocks LOW	- 2	0	+ 4	Volts	
$V_{\phi R}$ HIGH	Reset Gate Clock HIGH	+ 6	+ 10	+ 14	Volts	
$V_{\phi R}$ LOW	Reset Gate Clock LOW	- 4	0	+ 2	Volts	
$V_{\phi VTG}$ HIGH	Vertical Transfer Gate Clock HIGH	+ 5	+ 9	+ 15	Volts	
$V_{\phi VTG}$ LOW	Vertical Transfer Gate Clock LOW	- 2	0	+ 4	Volts	

AC CHARACTERISTICS: T_P = 25 °C (Note 1)						
SYMBOL	PARAMETER	RANGE			UNIT	CONDITION
		MIN	TYPICAL	MAX		
V_{ODC}	Output DC Level	13	16.4	19	Volts	Note 6
R_o	Output load Resistor	1.0	5.0	20	KΩ	
$f_{MAX\ HORIZ.}$	Horizontal Clock Frequency		5	10	MHz	
P_D	On-Chip Power Dissipation		1.0		W	Note 7

NOTES

1.- T_P is defined as the package temperature.

2.- Standard test conditions are nominal MPP clocks and DC operation voltages. 5.2 MHz horizontal data rate, integration time = 5.25 msec. Values shown are for 25 °C, unless otherwise indicated.

3.- Dark Current doubles every 5-7 ºC.

4.- Excluding spikes.

5.- Excluding spikes, and measured @ ½V_{sat}

6.- For the cases of V_{RD} = MIN, TYPICAL, MAX and R_o = 5 kΩ

7.- At f_{MAX} = 5 MHz, one On-Chip amplifier output, vertical & horizontal registers.

8.- Device has 4 On-Chip amplifier output options.

COSMETIC SPECIFICATION Maximum Allowable in:	COSMETIC GRADING CCD 485		
CENTRAL REGION	**1**	**2**	**3**
Value of X & Y	3	5	10
Defective Columns > 1 x Y pixels (Total)	12	24	40
Defective Rows > X x 1 pixels (Total)	12	24	40
Maximum Defective Cluster Size (X x Y)	3 x 3	5 x 5	10 x10
Defective Pixels (including Clusters, but excluding Col/Row defects)	400	600	1,200
Maximum Adjacent Defective Columns/Rows	3	4	5
Minimum number of good pixels between occurrences	4	4	2
OUTSIDE CENTRAL REGION			
Value of X & Y	3	5	10
Defective Columns > 1 x Y pixels (Total)	20	45	70
Defective Rows > X x 1 pixels (Total)	20	45	70
Maximum Defective Clusters Size	3 x 3	5 x 5	10 x 10
Defective Pixels, (including Clusters, but excluding Col/Row defects)	1,600	2,400	4,800
Maximum Adjacent Defective Columns/Rows	3	4	5
Adjacent Defective Columns/Rows per single occurrence	0	5	6,7,8,9,10
Minimum number of good pixels between occurrences	4	4	2

NOTES

1.- Cosmetic testing is done under uniform illumination . It is typically measured under ½ Vsat illumination. Consult Lockheed Martin Fairchild Systems for Custom Selections.

2.- Total number of clusters must contain ≤ the number of defective pixels allowed.

COSMETICS SPECIFICATIONS

DEFINITIONS:

Adjacent.- Neighboring and touching.

Active Pixel.- A pixel that is responsive to light or energy.

Central Zone.- The centered area of the total imaging area. For example, for CCD442A (2048 x 2048 pixels), the centered 1K x 1K coordinates are: $\{512 \leq (x, y) \leq 1512\}$. For a CCD485 & CCD481 (4096x4096 pixels), the centered 2K x 2K coordinates are: $\{1024 \leq (x, y) \leq 3072\}$.

Cluster.- A group of defective pixels.

Cluster Size: The area enclosing the group of defective pixels. The area dimensions are specified by the Cartesian coordinates of X x Y pixels. The length and width of "X &Y" are given in the *Cosmetic Specification* table for a specified device grade.

Column.- Any > 1 x Y consecutive pixels. The length of "Y" is given in the *Cosmetic Specification* table for a given device grade. Therefore, a section larger than 1 x Y in the vertical direction (following Cartesian coordinates) is considered a column. If smaller than 1 x Y, it is considered as a cluster.

Dead Pixel.- A pixel that fails to respond to light or energy.

Inactive Pixel.- A pixel that is not responsive to light or energy by design, such as dark reference pixels.

Outer Zone.- The area outside the central zone. For example: For CCD442A the outside surrounding a centered 1K x 1K coordinates are: $\{1 \leq (x, y) < 512\}$ & $\{1512 < (x, y) \leq 2048\}$. For CCD485 & CCD481 (4096 x 4096 pixels), the outside surrounding a centered 2K x 2K coordinates are: $\{1 \leq (x, y) < 1024\}$ & $\{3072 < (x, y) \leq 4096\}$.

Pixel.- One picture element of an imaging array.

Row.- Any > X x 1 consecutive pixels. The length of "X" is given in the *Cosmetic Specification* table for a given device grade. Therefore, a section larger than X x 1 in the horizontal direction (following Cartesian coordinates) it is considered a row. If smaller than X x 1, it is considered a cluster.

TYPE OF COSMETIC DEFECTS

Bright Columns/Rows/Clusters: Any Column/Row/Cluster that fails the PRNU specification and is ***brighter*** then the local average signal.

Column Shifts: A column (or group of columns) in which some or all of the pixels appear shifted up or down with respect to its adjacent columns. This phenomena is also known as "*weeping*". Column shifts are treated as defective columns.

Dark Columns/Rows/Clusters: Any Column/Row/Cluster that fails the PRNU specification and is ***darker*** then the local average signal.

Defective Pixel: Any pixel which fails the PRNU specification.

Defective Column: Any >1x Y consecutive defective pixels. The length of "Y" is given in the *Cosmetic Specification* table for a given device grade.

Defective Rows: Any > X x 1 consecutive defective pixels. The length of "X" is given in the *Cosmetic Specification* table for a given device grade .

Defective Cluster: Any group of defective pixels in which one or more pixels are contained outside the specified cluster size. Below is an example of a cluster rejected for a maximum cluster size of a 10 x 10 pixels size.

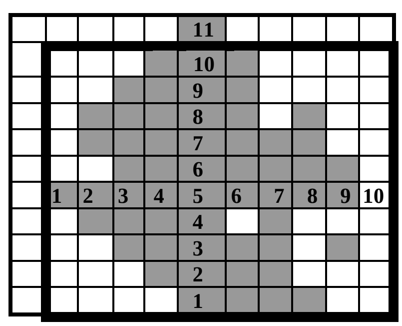


Fig. 1 Example of a defective 9 x 11 Cluster.

(this cluster will fail a maximum cluster size spec of 10 x 10 since one pixel extends outside the X x Y specified area. Total Bad Pixels = 56)

FOR INFORMATION ONLY:

Proximity Pixel/Col/Row/.- Correctable Pixel/Row/Col/defects that fall within the unallowable proximity to the next defect. (i.e. bad columns/rows that do not have the minimum distance allowable for the next defect, but they can be corrected and agree in quantity with the specification). For example, the minimum spacing allowed between defects is 5 pixels. Therefore if you have 2 bad columns separated by one good, it will fail if your spec allows you to have only 2 adjacent defective columns. Thus, it does not meet the spacing criteria. This example would be a "*proximity 2 columns*" and <u>not</u> adjacent 2 columns).

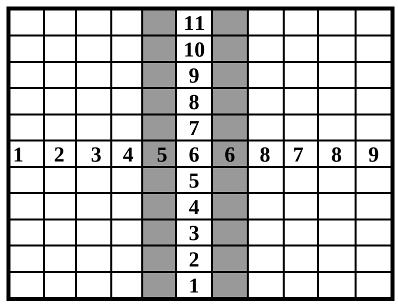


Fig. 1 Example of proximity 2 columns.

Stair Case Cluster: Pixels that fall outside the cluster size (X x Y), but have ≤ X x Y number of allowable bad pixels. The following examples illustrates its advantages.

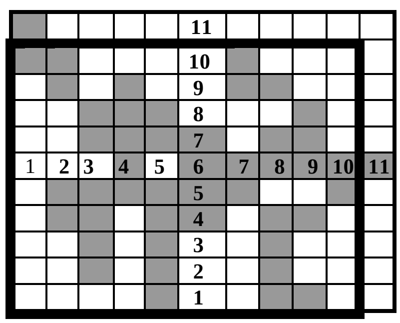


Fig. 2 Example of a Stair Case Cluster.

(this cluster would be rejected since two pixels extends outside the X x Y area : Total Bad Pixels = 47)

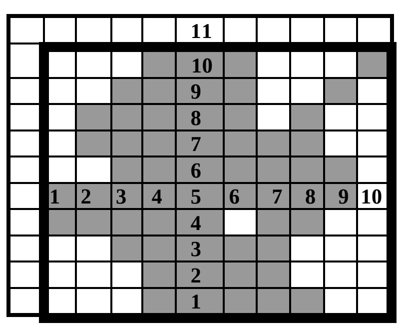
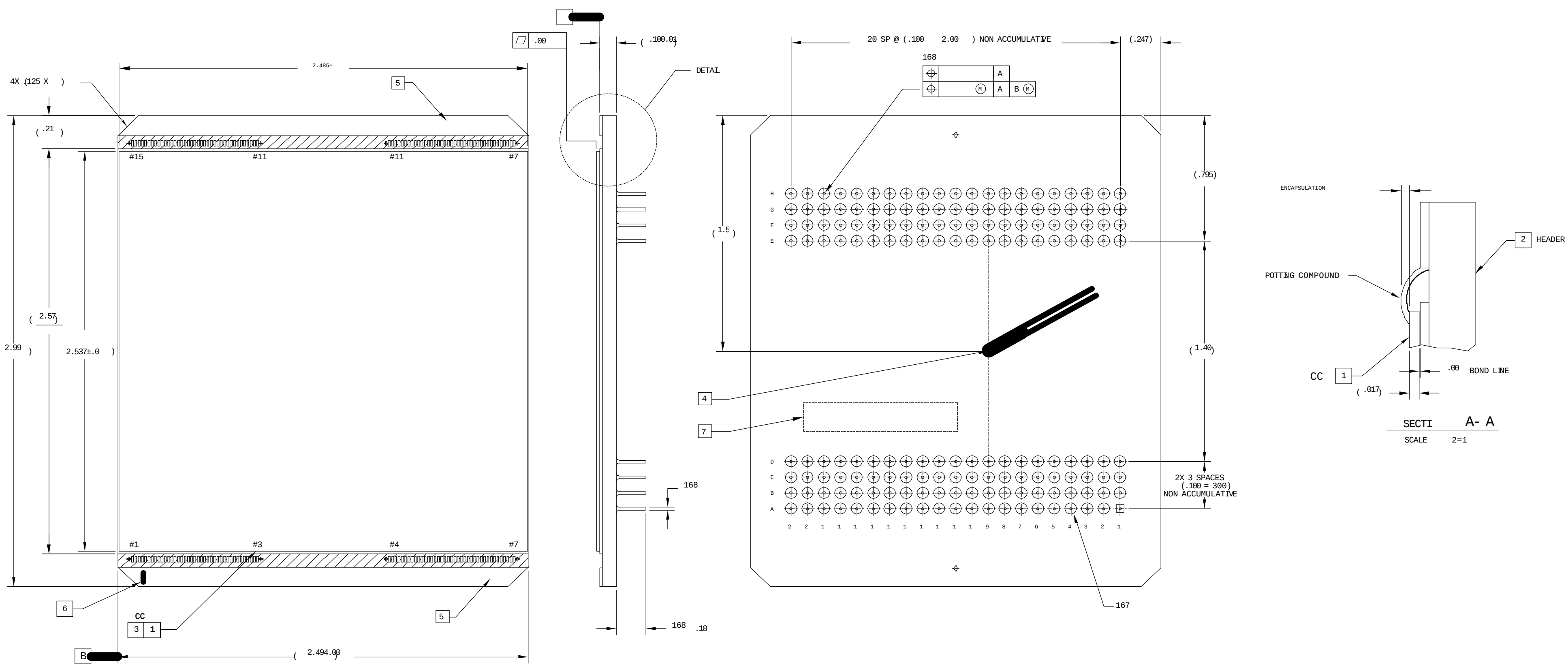
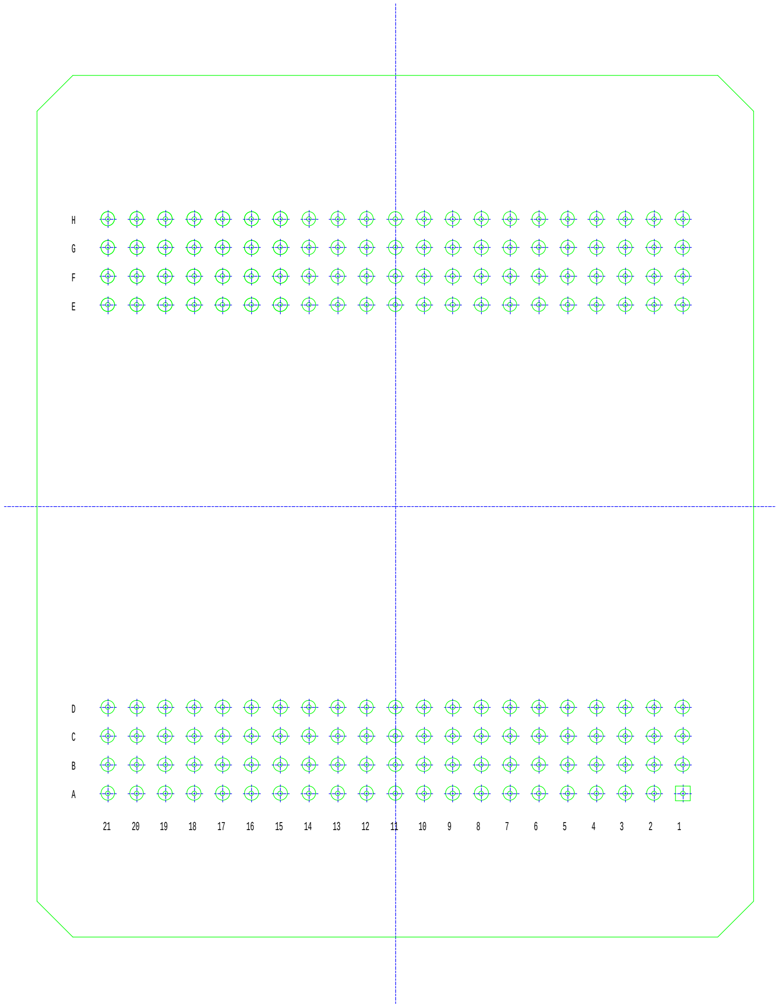


Fig. 3 Example of a Defective Cluster.

(this cluster would pass spec since no pixels extends outside the X x Y area : Total Bad Pixels = 59).



NOTES:	
① FOCAL PLANE ARRAY (CCD485)	
② HEADER	
③ CCD SHALL NOT OVERHANG SIDES OF HEADER	
④ TEMP SENSOR (OPTIONAL)	
⑤ SLIGHT CHIPPING US ALLOWED IN THIS AREA AS LONG AS FUNCTIONALITY IS UNAFFECTED	
⑥ MARK ARROW IS APPROXIMATE POSITION SHOWN TO INDICATE PIN # 1	
⑦ DEVICE IDENTIFICATION NUMBER (APPROXIMATE LOCATION)	
PACKAGING	ALUMINA TRIOXIDE (AL_2O_3) PIN GRID ARRAY (PGA)
PIN LENGTH	0.180 ” ± 0.020 ”



CCD485 PINOUT

	A	B	C	D	E	F	G	H
1	VDD_{UL}	VOG_{UL}	$H1_{UL}$	$H1_{UL}$	$H1_{UR}$	$H1_{UR}$	VOG_{UR}	VDD_{UR}
2	$Vout_{UL}$	ϕSG_{UL}	$H3_{UL}$	$H2_{UL}$	$H2_{UR}$	$H3_{UR}$	ϕSG_{UR}	$Vout_{UR}$
3	VRT_{UL}	$H3_{UL}$	$H2_{UL}$			$H2_{UR}$	$H3_{UR}$	VRT_{UR}
4	VRD_{UL}	ϕR_{UL}	ϕVTG_{UL}	Vss	Vss	ϕVTG_{UR}	ϕR_{UR}	VRD_{UR}
5	$V1_{UH}$	$V2_{UH}$	$V3_{UH}$	$V1_{UH}$	$V1_{UH}$	$V3_{UH}$	$V2_{UH}$	$V1_{UH}$
6	$V2_{UH}$	$V3_{UH}$	$V1_{UH}$	$V2_{UH}$	$V2_{UH}$	$V1_{UH}$	$V3_{UH}$	$V2_{UH}$
7	$V3_{UH}$	$V1_{UH}$	$V2_{UH}$	$V3_{UH}$	$V3_{UH}$	$V2_{UH}$	$V1_{UH}$	$V3_{UH}$
8	$V2_{UH}$	$V3_{UH}$	$V1_{UH}$	$V3_{UH}$	$V3_{UH}$	$V1_{UH}$	$V3_{UH}$	$V2_{UH}$
9	$V2_{UH}$	$V1_{UH}$	$V3_{UH}$	$V2_{UH}$	$V2_{UH}$	$V3_{UH}$	$V1_{UH}$	$V2_{UH}$
10	$V1_{UH}$	$V3_{UH}$	$V2_{UH}$	$V1_{UH}$	$V1_{UH}$	$V2_{UH}$	$V3_{UH}$	$V1_{UH}$
11	Vss	Vss	Vss	Vss	Vss	Vss	Vss	Vss
12	$V3_{LH}$	$V1_{LH}$	$V2_{LH}$	$V3_{LH}$	$V3_{LH}$	$V2_{LH}$	$V1_{LH}$	$V3_{LH}$
13	$V2_{LH}$	$V3_{LH}$	$V1_{LH}$	$V2_{LH}$	$V2_{LH}$	$V1_{LH}$	$V3_{LH}$	$V2_{LH}$
14	$V2_{LH}$	$V1_{LH}$	$V3_{LH}$	$V1_{LH}$	$V1_{LH}$	$V3_{LH}$	$V1_{LH}$	$V2_{LH}$
15	$V1_{LH}$	$V3_{LH}$	$V2_{LH}$	$V1_{LH}$	$V1_{LH}$	$V2_{LH}$	$V3_{LH}$	$V1_{LH}$
16	$V2_{LH}$	$V1_{LH}$	$V3_{LH}$	$V2_{LH}$	$V2_{LH}$	$V3_{LH}$	$V1_{LH}$	$V2_{LH}$
17	$V3_{LH}$	$V2_{LH}$	$V1_{LH}$	$V3_{LH}$	$V3_{LH}$	$V1_{LH}$	$V2_{LH}$	$V3_{LH}$
18	VRD_{LL}	ϕR_{LL}	ϕVTG_{LL}	Vss	Vss	ϕVTG_{LR}	ϕR_{LR}	VRD_{LR}
19	VRT_{LL}	$H3_{LL}$	$H2_{LL}$			$H2_{LR}$	$H3_{LR}$	VRT_{LR}
20	$Vout_{LL}$	ϕSG_{LL}	$H3_{LL}$	$H2_{LL}$	$H2_{LR}$	$H3_{LR}$	ϕSG_{LR}	$Vout_{LR}$
21	VDD_{LL}	VOG_{LL}	$H1_{LL}$	$H1_{LL}$	$H1_{LR}$	$H1_{LR}$	VOG_{LR}	VDD_{LR}

UL = Upper Left, LL = Lower Left, UR = Upper Right, LR = Lower Right, UH = Upper Half, LH = Lower Half